Libero SoC v11.8

Release Notes

09/2017

Microsemi

Power Matters.™

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at **www.microsemi.com**.

51300167-2/09.17

Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 2.7

Added Known Issues 3.1.35, 3.1.36.

Revision 2.6

Added Known Issues 3.1.33, 3.1.34. Added Resolved Issue – Export Flashpro Express Job tool crashes for particular use cases.

Revision 2.5

Added Resolved Issue – Programming SmartFusion2/IGLOO2: Incorrect SPI file generation and Programming Recovery settings erased.

Revision 2.4

Added Known Issue 3.1.32.

Revision 2.3

Added Resolved Issue for Customer Case 493642-2306065378, SAR 90123.

Revision 2.2

Added Known Issue 3.1.31.

Revision 2.1

Revision 2.1 includes fix for a critical Synplify bug and a description of its scope.

Revision 2.0

Revision 2.0 includes a critical Synplify bug fix and steps to follow to use the new Synplify Pro version.

Revision 1.0

Revision 1.0 is the first publication of this document.

Alert

This Alert is only for Windows users of Libero SoC. Linux users may disregard this alert.

A critical bug has been found in the Windows version of Synplify Pro included in the original Libero SoC release (uploaded 3/10/2017). Users who have downloaded Libero SoC v11.8 before 4:00am Pacific Daylight time (PDT), April 6, 2017, will be affected by this issue. You can tell if you are affected by this issue if:

- You try to invoke Synplify, or run Synthesis, and the tool does not launch or execute
- Your Libero installer's md5sum was:
    - *Web Install* setup.exe: 3ad69bb89938101753645b3a82bec78e
    - *Full Install* LiberoSoC_v11.8_Win.zip: 2e62a387a29c1a77fe4486e2cddbac31

You are **not** affected by this issue if you downloaded Libero SoC v11.8 after 4:00am PDT, April 6, 2017.

If you downloaded the beta version of Synplify (made available 3/29/2017), you do not need to take any action. This version has passed all tests and is now considered a production version of Synplify. You may continue using it as normal.

If you are still affected by this issue, follow these steps to use the updated version of Synplify Pro with your existing Libero SoC v11.8 install.

1. Download the Synplify Pro release from here.

2. Install Synplify Pro L2016.09M2_Beta to a new folder (different than the Synplify folder which is part of the Libero SoC v11.8 install).

3. Change the Libero SoC Tool Profile for Synthesis (**Libero SoC > Project > Tool Profiles > Synthesis**) to point to the location of the newly-installed Synplify Pro executable (in the Synplify install folder, "bin/synplify_pro.exe").

4. Ensure that the updated tool profile for Synthesis is set to be the Active profile (The Active radio button is checked).

Contents

Libero SoC v11.8 Release Notes

Microsemi Libero® System-on-Chip (SoC) design suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with Microsemi's power-efficient flash FPGAs, SoC FPGAs, and rad-tolerant FPGAs. The suite integrates industry-standard synthesis and simulation tools—Synopsys Synplify Pro® and Mentor Graphics ModelSim, respectively—with best-in-class constraints management, debug capabilities, and secure production programming solution.

Libero SoC v11.8 can be used for designing with Microsemi RTG4 Rad-Tolerant FPGAs, SmartFusion2 and SmartFusion® SoC FPGAs, IGLOO®2, IGLOO, ProASIC3®, and Fusion® FPGA families.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. Development Kits & Boards are listed in the **Design Resources** tab.

Contents

1 What's New in Libero 11.8

1.1 Silicon Features

No new silicon part is introduced with this release.

1.2 Software Enhancements

Unless otherwise noted, Software Enhancements apply to all SmartFusion2, IGLOO2, and RTG4 devices.

.

1.2.1 SmartDebug: FPGA Hardware Breakpoint, SRAM Logical View, Multiple Lane PRBS Test, Polling

The SmartDebug tool in Libero SoC v11.8 has been enhanced with significant new features.

FPGA Hardware Breakpoint (SmartFusion2 and IGLOO2) - You can automatically instantiate the FPGA Hardware Breakpoint (FHB) module into the user design. This feature is available in the Enhanced Constraint Flow only.

- FHB allows you to select any probe point (via Live-probe feedback) as a trigger to halt the design, and then single-step your design using SmartDebug.
- You can configure FHB to wait for up to 255 user clock cycles after the trigger event is detected before the user clock is halted. The trigger event occurs on the rising edge of the trigger signal selected by the user.
- SmartDebug allows you to:
  - o Capture and collect multiple snapshots using the **read_active_probe** Tcl command.
  - o Export a VCD waveform file of the selected signals. You can then review the waveform using any waveform viewer that supports VCD file format.
  - o Initialize the selected probe points by using the **write_active_probe** Tcl command or the Active Probe GUI before advancing the user clock.
- The FHB module instantiated by the tool includes the Event Counter and the Frequency Meter. The Event Counter is a 32-bit counter that keeps track of the number of times the rising edges have been detected on the selected probe point. The Frequency Meter estimates the frequency of the user clocks, as well as any selected probe points.

See the SmartDebug for Libero SoC v11.8 User Guide for details.

Fabric SRAM Memory Logical View – In addition to the physical view, SmartDebug now supports the logical view of LSRAM and uSRAM as defined by the user through inference from the flattened netlist.

Multiple Lane PRBS Test - You can run the same PRBS test on multiple lanes in a SERDES block.

Active Probe polling - This feature allows the tool to read iteratively a selected signal or bus until a specified value is read via Active Probe or a maximum count of iteration has been reached.

Runtime Improvements - Faster response time for Add/Delete Probes operations for very large designs.

1.2.2 SystemVerilog Support

Libero SoC v11.8 expands SystemVerilog support including:

- Importing SystemVerilog source (*.sv) files
- Importing files containing packages
- SmartDesign Instantiation Flow

1.2.3 ModelSim Microsemi Pro: Mixed Language Simulation and Improved Performance

Libero SoC v11.8 introduces a new simulator: ModelSim ME Pro that provides mixed language simulation for Verilog, SystemVerilog, and VHDL. This new edition of the simulator also provides enhanced runtime performance.

Libero SoC v11.8 offers both ModelSim ME 10.5c and ModelSim ME Pro 10.5c and both simulators are installed by default during installation. No manual set up is necessary to use ModelSim ME 10.5c, which is the default simulator.

To switch to ModelSim ME Pro 10.5c and use it as the default simulator:

- Change the tool profile (**Project > Tool Profiles > Simulation**) to point to the location of ModelSim ME Pro 10.5c

  - Windows
    <Libero_SoC_Install_folder>\ModelsimPro\win32acoem\modelsim.exe
  - Linux
    < Libero_SoC_Install_folder>/ModelsimPro/modeltech/linuxacoem/vsim

- Change the Simulation library location (**Project > Project Settings > Simulation Libraries)** to point to the precompiled simulation library location for ModelSim ME Pro.
- Existing Libero Gold or Platinum licenses can check out a ModelSim ME Pro license. Contact Corporate Technical Support at SoC_Tech@microsemi.com if there is a license checkout problem with a Libero Gold or Platinum license.
- For Platinum USB Dongle License users, a new dongle driver version (SCL_FLEXID9_Installer.exe) is required and available for download . See the Licensing downloads page for details.
- (For Floating License Only) Make sure that the lmgrd FLEXnet version is equal to or greater than 11.13.0.2. If not, download and install the lmgrd version from here.

1.2.4 Secure Production Programming Solution (SPPS): Design Security PUF Keys

Libero SoC v11.8 SPPS adds support for Design Security PUF Keys in M2S060, M2S090, M2S150, M2GL060, M2GL090 and M2GL150 devices.

- Factory PUF ECC key – enables secured production programming at contract manufacturing site without DFK database.
- User PUF AES key – User Encryption Key 3 (UEK3). This support is added to both SPPS and non-SPPS flow. The supported use cases are the same as the use cases in UEK1 and UEK2 in both flows. Similar to UEK1 and UEK2, UEK3 can be:
  - Provided by the user in the Security Policy Manager in Libero SoC
  - Used to encrypt the update bitstream when generating STAPL, SPI and DAT bitstream files.
  - Injected into the device at the same time UEK1 and UEK2 is programmed via SPPS or non-SPPS flow.

UEK3 is supported in Libero SoC, FlashPro Express and JobManager.

Note: DirectC support for UEK3 is not available and is planned for a future release.

1.2.5 New Tool - Netlist Viewer

Libero SoC v11.8 includes a new tool, the Netlist Viewer. This new tool provides Libero SoC users a graphical representation of the netlist for probing into the design at different stages of the design cycle. See Standalone Netlist Viewer User Guide for details.

The Netlist Viewer can be invoked in standalone mode from the Design Flow window. The standalone Netlist Viewer provides the pre-synthesis RTL view, the post-synthesis hierarchical view and the post-compile flattened view.

The Netlist Viewer is integrated in Chip Planner. The Netlist Viewer invoked from Chip Planner does not provide the RTL view and it can only be invoked after the synthesis step is completed.

1.2.6 Synplify Pro Microsemi Enhancements

Libero SoC v11.8 includes a new version of Synplify Pro ME (L2016.09M-2) with enhancements for SmartFusion2, IGLOO2 and RTG4:

- Infer Wide-mux hard macros
- Bus-aware replication of registers on select lines of Mux
- Pack enable signal with higher priority than sync-reset into SLE
- Logic reduction with tied inputs
- Infer Enable on address register of uSRAM
- RTG4 LSRAM: do not infer Feed-Through Write mode
- RTG4 Math: infer only one asynchronous reset

1.2.7 M2S/M2GL060T, M2S/GL090T– High Speed Serial Interface 3 PCIe L2P2_ACTIVE Signals

The PCIe L2P2_ACTIVE signals generated from High Speed Serial Interface 3 configurator for SmartFusion2 devices M2S060T and M2S090T, and IGLOO2 devices M2GL060T and M2GL090T are now triggered from the proper source. Update the version of SERDES_IF_3 core to 1.2.212 and re-generate the component before continuing with the design flow in Libero SoC v11.8.

1.2.8 SmartFusion2/IGLOO2 and RTG4 SgCore Changes

The following SgCores have been updated to be compatible with Libero v11.8. If an existing project contains any of the following cores, update the core to the latest version and regenerate the component before continuing with the design flow in Libero SoC v11.8.

Core	Family	Device	Libero SoC v11.8 Compatible Version	Changes
SERDES_IF_3	SmartFusion2	M2S060T M2S090T	1.2.212	PCIe L2P2_ACTIVE signals
	IGLOO2	M2GL060T M2GL090T		
RTG4FCCC	RTG4	RT4G150	1.1.217	Hold violation on Dynamic CCC on APB_S_PSEL and APB_S_PADDR paths
RTG4CCCAPB_IF	RTG4	RT4G150	1.1.106	

1.2.9   Globals Placer Optimization of CCC Placement

The Globals placer for SmartFusion2, IGLOO2 and RTG4 in Libero SoC v11.8 optimizes the placement of CCC instances to reduce the distance from their fixed drivers (oscillator, I/O or logic).

1.2.10 XAUI Protocol – Edit Registers List

The High-speed Serial configurators for SmartFusion2, IGLOO2 and RTG4 in Libero SoC v11.8 show all the advanced registers relevant for the XAUI protocol in the Edit Registers list.

1.2.11 RTG4 Global Net Report – Clocks and Resets not Radiation Protected

The Global Net Report for RTG4 designs in Libero SoC v11.8 appends a new Warning section that lists all clock nets and asynchronous reset/preset nets, the implementation of which may not be protected from radiation upsets.

1.2.12 RTG4 CCC – Simulation Runtime Improvement

The CCC simulation model for RTG4 designs in Libero SoC v11.8 has been optimized to run up to three times faster.

1.2.13 RTG4 Single Event Transient (SET) Mitigation – Option Location Change

The Single Event Transient (SET) Mitigation option for RTG4 designs has been relocated to the Device Settings window of the New Project Wizard (**Project > New Projects**) and the Project Settings dialog box (**Project > Project Settings**).

1.2.14 Enhanced Constraint Flow

The Libero SoC Enhanced Constraint Flow, first introduced in Libero SoC v11.7, has been improved with the following:

- Design Block Flow is added. With this addition, both the Libero SoC Enhanced Constraint Flow and the Libero SoC Classic Constraint Flow support the creation and import of design blocks for use in a bottom-up design methodology. See SmartFusion2, IGLOO2, and RTG4 Designing with Blocks for Libero SoC 11.8 in Enhanced Constraint Flow for details.

- The I/O Advisor tool has been integrated into the Constraint Manager. To invoke the I/O Advisor for the Libero SoC Enhanced Constraint Flow, double-click Manage Constraints in the Design Flow window, select I/O Attributes, Click Edit and select Edit with I/O Advisor (**Design Flow window > Manage Constraints > I/O Attributes > Edit > Edit with I/O Advisor**).

  Note: For Classic Constraint Flow users, there is no change. Invoke the I/O Advisor from the Design Flow window.

1.2.15 Changes to Libero SoC and DirectCore Licensing Options

Libero SoC v11.8 introduces two new free license options – Evaluation and Silver. The following changes in licensing options are being rolled out.

- The free Evaluation license supports all devices for software evaluation, but does not include programming or debug tools.
- The free Silver license supports smaller density devices and includes ModelSim ME.
- The Gold license is now a paid license and supports the largest FPGA Flash-based devices, all kit devices, and includes ModelSim ME and ModelSim ME Pro simulators.

- The Platinum license remains a paid license, supports all devices, and includes ModelSim ME and ModelSim ME Pro simulators.
- A Standalone license supports all devices and is for users who have their own Synthesis and Simulation tools for Microsemi devices.
- A few free RTL source DirectCore IPs are moved to paid Libero licenses.

Customer Notification CN17012 tabulates the features for each license types.

1.2.16 ProASIC3, IGLOO, Fusion, SmartFusion – SRAM Configurations Depth-wise

Libero SoC v11.8 updates both two-port and Dual-port SRAM configurators for ProASIC3, IGLOO, Fusion and SmartFusion to address the following issues.

- **Two-port SRAM configurations of multiple blocks depth-wise and dynamic REN signal**. When the REN is de-asserted and the read address jumps from one block to another block, the read-data is not held.
- **Dual-port RAM configurations of multiple blocks depth-wise and dynamic BLKA or BLKB signal**. When the BLKA or BLKB is de-asserted and the corresponding port address jumps from one block to another block, the port's read-data is not held.

1.2.17 New Operating System Support

Libero SoC v11.8 adds support for the following operating systems:

- Windows 10
- RHEL 7
- CentOS 7

2 Resolved Issues

The following table lists the customer-reported SARS resolved in Libero SoC v11.8.

Customer Case Number	Description
493642-2046740027	Generating a SVF file with only Erase and Program Array using Designer
493642-2195062181	G4 programming recovery failure when power cut at certain times
493642-2166423130	STAPL JESD71 Standard
493642-2121872068	Programming fails with IDE9.1 PDB file but passes with IDE9.1 STP
493642-2007160699	Improve options naming under Debug security policy (SF2)
493642-1996472989	Backlevel Protection in Update Policy should give some information once enabled
493642-2105539941	Deasserted TPSRAM REN or DPSRAM BLKA/B doesn't hold read-data when address jumps into another block
493642-2208341335	XAUI IP configuration registers overlay some PCIe configuration registers
493642-2137035639	SERDES_IF3 PCIe L2P2_ACTIVE signaling is assigned to EPCS_2_RXCLK_net
493642-2212077616	RTG4 High Speed Serial Interface is not retaining ODT settings when we reopen the configurator
493642-2089019331	Micro SRAM GUI configurator: disable clocks when unused.
493642-2163132355	uPROM simulation fails due to space in mem file path name
493642-2039633013	Update SB Security > master/slave tab for S device and in Security configurator.
493642-2161854133	Documentation: Improve Info message in log window about ambiguities in clock network
493642-2123365449	Documentation: Enhanced Constraint flow doesn't have "Compile" option; need to correct the Manual
493642-2021863238	Documentation: "RAM with init" SmartGen block is supported only for Fusion.

493642-2176234833	Documentation: DDR configurator outputs RESET_n signal for LPDDR and DDR2 memories which is wrong
493642-2167713748	Documentation: clock_fall is not supported for set_clock_to_output. Please remove it
493642-2123141885	Documentation: Cache option is available in the MSS EDAC configuration user guide
493642-1843877113	Documentation: Debug Security Policy help is not complete
493642-2193779760	Dynamic configuration of CCC is failing in simulation.
493642-2088495825	IOBAG4: Layout should automatically use the SE0 or SE1 CCC/PLL locations when connecting from RCOSC
493642-2150390432	Modify serialization client GUI not accepting HEX Input
493642-1506975832, 493642-1609820607, 493642-1622538232	Export Active Probe and Memory content from GUI to file
493642-2164407086	SmartDesign instance HDL background auto-checker
493642-1855329920	Signals named "Warning" and "Error" in design show as a Warning and Error message in Timing report
493642-2114634116	Manage Suppressed Messages are losing the Messages ID if the project is closed and reopened
493642-2005356442	Libero editor fails to warn when saving to a read only file
493642-1967812567	Make the message window active when errors are generated
493642-194278428	SmartDesign: Enhancement request to provide an option to re-name the core once it is configured.
493642-2163038251	Cycle accurate: Importing a VCD causes crash in SmartPower
493642-2214820736	Disable Generate DAT files for RTG4 family of devices. (DEF)
493642-2049170760	A problem with design hierarchy when the Component instantiation is done in a different way
493642-1977246176	Libero only includes use clause statement that ends with ".all" in Synplify Pro Prj file
493642-1906361072	HDL port data type changes to STD_Logic after Block Creation
493642-2114579112,493642-2120954795	Add SystemVerilog support to Libero
493642-2105665350,493642-	Tcl script to launch ModelSim interactively in batch mode

2117472239	
493642-1816608745	Block created doesn't include the Bus interface signals
493642-2202430624	Synplify Pro is creating wrong Math block implementation
493642-2193090274	Synplify Pro error during Compile in Libero v11.7.
493642-2137453331	Documentation: Synplify Pro updates Microsemi SmartFusion2 MACC Blocks inference with RTG4 support
493642-2138676997	Synplify Pro inferring RAM throws error and crashes.
493642-2128744071	Synplify Pro long run time with J2015 release
493642-2118765487	Synplify Pro gives @E: : | Internal Error in c_vhdl.exe
493642-2106946439	Synplify Pro replicates the CLKINT_PRESERVE macro
493642-1984004911	Synplify Pro: RAM not inferred when used with "uSRAM" or "LSRAM" attribute
493642-1877536469	Synplify Pro: syn_ramstyle=block_ram is used but tool infers registers in the design.
493642-1831129078	Synplify Pro takes hours on a simple shift register design
493642-2237476292	RTG4 routing open failure for async-reset driven from GB in the presence of RCLKINT
493642-2162176960	CHIP_PLANNER: UNPLACED_MACROS: Min-Delay Repair Buffers show as unplaced in post-layout
493642-2142223664	Netlist Viewer is not available in Enhanced Constraint Flow
493642-2023855057,493642-2160629194,493642-2229096786	SmartPower always sets VPP as 2.5
493642-2094000977	Global Net Report: RTG4 CCC report naming convention is showing PADN if more than one CCC is instantiated
493642-2072395998/493642-2011990594	Support for write count threshold check in SVF
493642-2102623482	Change FP5 Vpump detection level to match with FP4
493642-2246593390	A multi-pass P&R job does not stop with the Stop button
493642-2306065378	The application cannot start because its side by side configuration is incorrect
	Documentation: Remove any reference to CoreSF2Reset and CoreSF2Config cores and replace with CoreResetP and CoreConfigP
	UJTAG change to support Dual Use case

	Add a phrase in the menu to indicate JTAG mode only
	SPPS: JobManager needs to add support for eNVM placeholder clients
	SPPS: Add TCL to delete ticket by its ID for all SPPS flows (including IHP)
	Documentation: Which IEEE Standards are supported
	Design hierarchy: issue parsing VHDL libraries
	TCL command to output the Libero version in use
	Active Probe/Live Probe does not work on M2GL150 design/device
	Block flow (Classic) creates a wrong netlist for pre-layout Timer in 11.7 SP1 and later
	Active Probe : Allow multiple writes of same value to same signal
	Need to add sorting capability to probe insertion selected nets
	Porting from 11.6: Need to manually generate Programming and Debug file generation
	Documentation: All users MUST have write permission to the vault location
	Synplify Pro RTL view crashes with out of memory
	Synplify Pro: Confusing port name of Instantiated pad
	TEXT_EDITOR : Uncomment selection is not working
	Simulation: Combine vlog and vhdl precompiled libraries
	Project Description information is removed from prjx file
	Synplify Pro crashing with get_pins on RTG4 CCC
	RTG4 – SpaceWire Channels may Result in Hold Violations
	RTG4 – Single Event Transient (SET) Mitigation Option Change Does Not Revert Design to Pre-Compile/Pre-Synthesis State
	SmartFusion2, IGLOO2 and RTG4 – Slack mismatch in SmartTime – Path list vs. Expanded paths
	SmartFusion2/IGLOO2/RTG4 – Chip Planner Displays Some Unplaced Macros after Layout in Enhanced Constraint Flow and Minimum Delay Violations Repair
	SmartFusion2, IGLOO2, and RTG4 -Enhanced Constraint

	Flow Limitations – I/O Advisor, Netlist Viewer, Block flow
	Active Probe: Reading a single or multiple probe points from the same bus returns the entire bus value
	Bitstream Generation: Fails when clients are of type Memory File and content is filled with zeros.
	RTG4: UPROM CFG file parser causes Update UPROM client to crash
	SmartFusion2/IGLOO2: Incorrect SPI file generation and Programming Recovery settings erased when STP and DAT bitstream formats are exported together with SPI.
	Export Flashpro Express Job tool crashes for particular use cases

3 Known Limitations, Issues and Workarounds

3.1.1 SmartFusion2/IGLOO2 and RTG4 – SmartDebug Error when Probe Points Exceeds 1000

When more than 1000 probe points belonging to a bus are selected from the Hierarchical view and added to the Live/Active Probes tab, SmartDebug issues SQL error: "Expression tree is too large (maximum depth 1000)".

3.1.2 SmartDebug – Logical View for LSRAM/uSRAM Known Issues

The following SmartDebug known issues will be fixed in the next release.

- Logical view cannot be reconstructed for LSRAM/uSRAM for port widths of x1 inferred through RTL.
- Logical view cannot be reconstructed for LSRAM/uSRAM configurations when a single net of output bus is used i.e. A_DOUT[0]/B_DOUT[0] for DPSRAM/uSRAM and RD[0] for TPSRAM and others are unused. The memories can be read/write using physical view.
- Logical view cannot be reconstructed for LSRAM/uSRAM configurations inferred using IP Cores CoreAHBLtoAXI (Verilog flow), CoreFIFO (Verilog and VHDL flow).
- When the number of LSRAM/uSRAM blocks used for one logical ram block exceeds 10, the logical view constructed for the corresponding block is incorrect.

3.1.3 SmartDebug – FPGA Hardware Breakpoint (FHB) Auto Instantiation Limitations

- Support is limited to SmartFusion2 and IGLOO2 devices in Enhanced Constraint Flow only.
- Support is limited to FABCCC driven gated clocks.
- There is no support for EDIF flow and designs having Encrypted IPs.
- Live Probe triggering occurs on the Positive Edge only.
- When a signal connected to logic zero/ground (1'b0) is used as the live probe trigger, disarming the trigger leads to forced halt of DUT.
- FHB auto instantiation feature is not supported for block flow.

3.1.4 Synplify Pro Incorrectly Removes Inverters

Synplify Pro incorrectly removes inverters and generates incorrect output when all of the following are true:

1. A find command is used in the FDC file to get the collection of nets based on fanout values, e.g.

   ```
   define_scope_collection {fanout24} {find -hier -net {*} -filter \
   {@fanout > 24}}
   define attribute {$fanout24} {syn_maxfan} {24}
   ```

2. The RTL has some constants which should be propagated across inverters in the netlist

3.1.5 Standalone Netlist Viewer Known Issues/Limitations

The following are known issues/limitations for the standalone Netlist Viewer (**Design Flow > Implement Design > Netlist Viewer**):

- Runtime Penalty – Opening the flattened view of a large design on certain devices/packages may incur some runtime penalty. It may take a few minutes for the Netlist Viewer to display the flattened view.

- Memory issues –The tool may fail to open the flattened view of a large design on SmartFusion2/IGLOO2 150 devices (M2S/GL150) due to insufficient memory. For SmartFusion2/IGLOO2 090 devices (M2S/GL090), insufficient memory may prevent the Netlist Viewer from opening multiple netlist views if the page-splitting feature is disabled.

- All view buttons (RTL, Hierarchical Post-Synthesis, Flat Post-Compile) in Netlist Viewer may be de-activated (grayed-out) when the project path contains empty spaces.

- The Netlist Viewer cannot open the RTL view when there is a mix of VHDL and Verilog in the RTL codes.

3.1.6 SmartFusion2/IGLOO2/RTG4 Enhanced Constraint Flow and Fixed CCC Placement

When an instance of a Clock Conditioning Circuitry (CCC) is fixed in the Enhanced Constraint Flow, the Place and Route tool may error out if any of its hardwired inputs or outputs is also fixed into an incompatible location.

Workaround:
1. Unplace the CCC instance in Chip Planner or a pdc constraint file.
2. Rerun the Place and Route tool.

3.1.7 File > Print option in RedHat/CentOS 7.0 causes crashes

The File > Print option to print a report or a design file may cause Libero to crash on RedHat/CentOS 7.0.

3.1.8 Command "set_programming_action" fails during Programming of ProASIC devices

When a ProASIC3 device is programmed in Designer, the error "A programming file must be loaded before running the command **set_programming_action"** appears.

Workaround:
1. Export the PDB/STAPL file.
2. Open FlashPro and load the programming file to run programming.

3.1.9 RT4G150 352-CQFP Features

For the 352-CQFP package for RT4G150, programming is not enabled, timing numbers are in advance, and package power and design-specific IBIS and BSDL model details are not yet available.

3.1.10 Project Creation Wizard Online Help

When there is no project opened in Libero, the Project Creation Wizard Online Help cannot open the following online help topics:

- New Project > Device Selection > Help

- New Project > Device Settings > Help

- New Project > Design Template > Help

- New Project > Add Constraints > Help

3.1.11 Windows 10 and Window 8 Online Help for Configuration Cores

On windows 8/10 machines, the help link to User Guides for the following cores cannot be opened:

- Tamper2/3 cores

- High Speed Serial Interface 2/3 cores

- Clock Conditioning Circuitry (CCC) core

3.1.12 RTG4 - SmartDebug: Device Resets during JTAG Operations with SmartDebug

After performing one or more JTAG operations, if a user closes and reopens the SmartDebug tool (either standalone or within the Libero SoC software), the device resets itself.

Workaround:

The device reset problem can be avoided by using the FlashPro5 programmer and setting a value of 1 on the def variable **SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET.**

- For standalone SmartDebug:

  o When invoking the tool from the command line, add the following argument:

    Console >

    ./sdebug.exe **SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET**:1

  o When invoking the tool from the GUI, edit the sdebug.def file and change the value of def variable to '1' in the line below:

    data SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET 0 OVERRIDE

- For SmartDebug invoked from Libero SoC:

  o Edit the sdbg.def file and change the value of def variable to "1" in the line below:

    data SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET 0 OVERRIDE

  o Add the following line in the libero.def file:

    data SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET 1 OVERRIDE

- For Tcl script-driven batch mode operation, add the following def variable and the value in a Tcl script:

    defvar_set -name **SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET** -value 1

Note: When the def variable is set to 1, the LiveProbe set in the previous SmartDebug session is not retained when a subsequent SmartDebug session is invoked.

3.1.13 RTG4 - Custom Flow with uPROM: uPROM Content must be a Single Line File

If you use the custom flow and import the uPROM content using the import_component_data command, the uPROM memory file must not have any newlines.

3.1.14 SmartFusion2, IGLOO2 and RTG4 – Place and Route Tool does not Support get_nets or get_clocks SDC Commands

The placer does not support the get_nets and get_clocks object access commands when used with SDC timing constraints. To ensure that the SDC timing constraints are honored by the placer tool, do not use get_nets or get_clocks commands in the SDC timing constraints.

Workaround:

Use the get_pins command instead.

Example:

The following constraint uses the get_nets command:

```
create_generated_clock -name {sys_clk} -divide_by 1 -source [ get_ports { CLK_40M } ] -
phase 0 [ get_nets { u_PLL/my_pll_0/GL0_net } ]
```

Rewrite the constraint to use the get_pins command instead:

```
create_generated_clock -name {sys_clk} -divide_by 1 -source [ get_ports { CLK_40M } ] -
phase 0 [ get_pins { u_PLL/my_pll_0/CCC_INST/GL0 } ]
```

3.1.15 RTG4 -Single Event Transient (SET) Mitigation ON may Result in Hold Violations

Turning SET Mitigation ON may result in hold time violations in some register-to-MATH block paths. Enable Repair Minimum Delay Violations in Place and Route options to have the Place and Route tool mitigate hold time violations.

3.1.16 SmartFusion2/IGLOO2/RTG4 - Chip Planner Displays Some Unplaced Macros after Layout in Enhanced Constraint Flow

This is a Chip Planner display issue. It can be ignored if layout is successful.

- If nets on Row Globals or local asynchronous resets for RTG4 are constrained to a user-created exclusive region in Chip Planner before layout is run, re-opening Chip Planner may display the macros connected to those constrained nets as unplaced macros even though the layout process has successfully completed.

3.1.17 SmartFusion2, IGLOO2, and RTG4 - Enhanced Constraint Flow Limitations

The following tools and flows are not supported in the Enhanced Constraint Flow in the Libero SoC v11.8 release:

- Precision synthesis
- Design Separation Flow using MSVT

3.1.18 Extra Pop-Up Messages from Synplify Pro

When Synplify Pro synthesis is invoked interactively, it displays a pop-up message about the completion of Tcl script file execution, if any one of the following is true prior to the interactive invocation of Synplify Pro. Ignore the messages and click OK to continue with the Synplify Pro synthesis.

- Additional user-specified synthesis options are configured in a Tcl script and passed by Libero SoC to Synplify Pro.
- The Synthesis Option is entered in the Configure Synthesis Option dialog box as a command line entry and passed to Synplify Pro.

3.1.19 Programming - Libero SoC Crashes when Exporting FlashPro Express Job for UEK1 or UEK2 with eNVM

Libero SoC crashes when the Export FlashPro Express Job tool is invoked to generate a programming job encrypted using UEK1/UEK2 where eNVM is the only selected component.

Workaround:

Select both fabric and eNVM components for exporting the programming job encrypted using UEK1 or UEK2.

3.1.20 Programming - SPPS Flow: export_hsmtask fails when set_security_overwrite is followed by set_envm_update

If the user Tcl script has the security overwrite command followed by the eNVM update command, the export of the HSM job fails. In other words, if set_security_overwrite is followed by set_envm_update, the export_hsmtask fails.

Workaround:

If both the security overwrite command and the eNVM update command are required, make sure that the eNVM update command is executed prior to the security overwrite command. Put the set_envm_update Tcl command before the set_security_overwrite Tcl command in the Tcl script.

3.1.21 Programming - No Programming Support for Virtual Machines

Programming is supported for physical machines only and not supported on any virtual machine (VM).

3.1.22 Programming - Inspect Device Feature Disabled in FlashPro

The Inspect Device feature is disabled in FlashPro for SmartFusion2/IGLOO2 devices beginning with the Libero SoC v11.7 release. Use standalone SmartDebug instead.

3.1.23 Programming - SmartFusion Encrypted STP File Generation

Generating the encrypted STP files for SmartFusion takes 50 times longer than generating the non-encrypted plain STP.

3.1.24 ProASIC3 Devices Programming Action Failed

When programming a ProASIC3 device, the message "Error: A programming file must be loaded before running the command **set_program_action**" appears.

Workaround:

1. Export the PDB/STAPL file from Libero.
2. Open FlashPro and load the programming file to run programming.

3.1.25 SoftConsole - Restricts ARM® Cortex®-M3 Debug with Debug Pass Key

SoftConsole does not support this feature.

3.1.26 Documentation - Web-based Documentation

Starting with the Libero SoC v11.7 release, most users guides for SmartFusion2, IGLOO2, and RTG4 are available on the Microsemi website. Libero SoC and Programming/Debug tools include links to the website.

If the machine on which the Libero SoC software is installed does not have access to the internet, you (or a site administrator) can download all the Libero SoC v11.7 user guides from the Libero SoC documentation site.

3.1.27 Documents on Linux: Firefox Requirement for Online Help and User Guides

Libero SoC v11.8 requires the "Firefox" executable to be in your PATH variable on Linux. Alternatively, you can access the reference manuals on the Microsemi website, or by clicking **Help > Reference Manuals** in Libero SoC. For the Libero SoC SoC v11.8 release, the "Web Browser"

selection in the Libero SoC Preferences dialog box is only used by online help and for some user guide links.

3.1.28 Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines, the InstallShield wizard displays a pop-up message stating:

The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Click **Yes** to complete the installation.

3.1.29 Antivirus Software Interaction

Many antivirus and host-based intrusion prevention system (HIPS) tools flag executables and prevent them from running. To eliminate this problem, users must modify their security settings by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for assistance.

Many users are running Libero SoC successfully with no modification to their antivirus software. Symantec, McAfee, Avira, Sophos, and Avast tools have known issues. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC, ModelSim ME, and/or Synplify Pro ME may or may not be affected.

3.1.30 Installation Issue on Linux

After installation of Libero SoC on Linux, the attempt to run the udev_install script for FlashPro setup fails with the following message:

```
% ./udev_install
/bin/sh^M: bad interpreter: No such file or directory
```

Problem:

The script uses Windows CR/LF line termination instead of UNIX/Linux LF only line termination and, hence, is not a valid shell script.

Workaround:

Run the `dos2unix` command on the script to convert CR/LF line termination to LF only line termination:

```
% dos2unix udev_install
%. /udev_install
```

If the `dos2unix` command is not available, install the command first, and then run `dos2unix`, and udev_install:

```
% sudo yum install dos2unix
% dos2unix udev_install
%. /udev_install
```

3.1.31 Warning Message During Bitstream Generation/Programming

A warning message "Untested Windows version 6.2 detected!" appears on the Libero SoC Log window during Bitstream Generation on Windows 8 and Windows 10 machines. This warning

message originates from the Qt Library on which the bitstream generation tool is based. This message is benign and can be safely ignored.

3.1.32 SSN Results Not For Silicon Sign-Off

Simultaneous Switching Noise (SSN) is a noise analysis tool for SmartFusion2 and IGLOO2. The noise margin reported by the SSN Analyzer is computed based on the I/O standards, Drive Strength, and placement of the pin. The SSN Analyzer provides a general guideline and helps the designer to achieve the desired voltage noise margin. It is not intended to be used as a silicon sign-off tool.

3.1.33 Incorrect SPI file generated when using Update Policy

For Libero and Job Manager v11.8 and older, when Fabric/eNVM is protected with FlashLock/UPK1 in Update Policy in Security Policy Manager and SPI UEK1/UEK2/UEK3 bitstream files are exported, the SPI file will include Fabric/eNVM, even if they are protected in Update Policy. This generated UEK SPI bitstream file will fail programming, because there is no way to match UPK1 in SPI use models.

Workaround:

Do not export Fabric/eNVM in UEK1/UEK2/UEK3 SPI bitstream files if they are protected in Update Policy.

3.1.34 SmartDebug - Probe Insertion Flow: Router fails when nets are assigned to user locked I/Os

Probe insertion flow fails when a net is assigned to user I/O that is already locked.

3.1.35 Programming - The command set_programming_action fails

The command set_programming_action fails if a programming file is not loaded before running the command.

Workaround:

1. Export PDB/STAPL file.

2. Open FlashPro and load programming file to run programming.

3.1.36 Programming - eNVM with serialization only crashes during bitstream generation (SmartFusion2 and IGLOO2)

An eNVM design with only a serialization client causes a crash during bitstream generation.

Workaround:

1. Add a dummy "Data Storage" client.

2. Fill it with 0's.

3. Generate/export bitstream.

4 System Requirements

For information about operating system support and minimum system requirements, see the System Requirements web page.

Note: A 64-bit OS is required for designing with SmartFusion2, IGLOO2, and RTG4 devices.

For Linux OS setup instructions, see the Libero SoC Documents web page.

4.1.1 Operating System Support

Supported

- Windows 7, Windows 8.1, Windows 10*
- RHEL 5** and RHEL 6, , RHEL 7* , CentOS 5**, and CentOS 6, and CentOS 7*
- SuSE 11 SP4 (Libero only. FlashPro Express, SmartDebug, and Job Manager are not supported.)

 Note: * New OS support for this release.

   ** RHEL 5 and CentOS 5 do not support programming using FlashPro5.

Not Supported

- 32-bit operating system
- Windows XP
- Support for the following operating systems will cease in the second half of 2017:

    o RedHat Enterprise Linux 5.x through 6.5
    o CentOS 5.x through 6.5

5 Synopsys and Mentor Graphics Tools

Libero SoC v11.8 includes the following tools:

- Synplify Pro L2016.09M-2
- ModelSim ME 10.5c
- ModelSim ME Pro 10.5c
- Identify L2016.09M-2

6 Libero SoC v11.8 Download

Click the following links to download Libero SoC v11.8 on Windows and Linux operating systems:

- Windows Download
- Linux Download

Note: Installation requires administrator privileges to the system.

6.1 Downloading SoftConsole 3.4/4.0

Libero SoC v11.8 is compatible with SoftConsole v3.4 SP1 and SoftConsole v4.0. The following links contain the download packages, and explain the steps for downloading SoftConsole on different operating systems:

- Download SoftConsole v4.0 for Windows
- Download SoftConsole v4.0 for Linux
- Download SoftConsole v3.4 SP1 for Windows